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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,776	11/13/2003	Alok Kumar	10559-878001 / P17397	8759

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EXAMINER	
SAVLA, ARPAN P	
ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,776	KUMAR, ALOK	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/713776 has a total of 32 claims pending in the application, there are 6 independent claims and 26 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted are acceptable for examination purposes.

OBJECTIONS

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Allocating Content Addressable Memory (CAM) To A Microblock Of Instructions."

The disclosure is objected to because of the following informalities: The specification is objected to as failing to provide proper antecedent basis for the claimed

subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claims 11-20 recite a computer program, tangibly embodied in an information carrier, however, Applicant's specification does not define what this "information carrier" specifically entails.

Appropriate correction is required.

Claims

4. **Claim 26 is objected to because of the following informalities:**

The claim recites the limitation "the network processor" in line 1. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending the claim to read "the packet processor" in line 1.

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 11-20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** Claim 11 recites "a computer program product tangibly embodied in an information carrier, the computer program product being operable to cause a machine to...". However, because Applicant's specification does not define what this "information carrier" specifically entails it appears

to Examiner that the "information carrier" is an electrical signal, thus non-statutory subject matter.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** The phrase "capable of allocating" in claims 24 and 27 does not clearly identify if the "memory entry in a memory device" is actually allocated to the instructions or not. Also, the phrase "capable of maintaining" in claims 25 and 28 does not clearly identify if the "processor" is actually maintaining a "count of threads" or not. Finally, the phrase "capable of maintaining" in claims 26 and 29 does not clearly identify if "processor" is actually maintaining a "bit" or not.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 11, 21, 24, 27, and 30 are rejected under 35 U.S.C. 103(a) as being obvious over Aipperspach et al. (U.S. Patent 5,778,243) in view of Ramakrishnan (U.S. Patent 6,615,311).

11. **As per claims 1 and 11**, Aipperspach discloses a method comprising:

allocating a memory entry in a memory device to instructions executed on a multithreaded engine (col. 1, lines 33-40; col. 3, lines 44-47; col. 5, lines 31-32; Fig. 3). It should be noted that computer program product in claims 11-20 executes the exact same functions as the methods in claims 1-10. Therefore, any reference that teaches claims 1-10 also teaches the corresponding claims 11-20. It should also be noted that "processor" is analogous to "engine."

Aipperspach does not expressly disclose a packet processor and a portion of the memory entry includes a unique identifier assigned to the instructions.

Ramakrishnan discloses a packet processor and a portion of the memory entry includes a unique identifier assigned to the instructions (col. 4, lines 21-22 and 52-61; Fig.1, element 106; Fig. 2, element 220). It should be noted that "prefix entry mask word" is analogous to "unique identifier." It should also be noted that the "prefix entry mask word" associates the number of bits needed for a match between a CAM entry and its assigned instruction.

Aipperspach and Ramakrishnan are analogous art because they are from the same field of endeavor, that being memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Ramakrishnan's prefix entry mask word within Aipperspach's

memory entry as well embed Aipperspach's multi-threaded processor within Ramakrishnan's packet processor.

The motivation for doing so would have been to conserve CPU memory when updating CAM entries by not having to maintain a bitmap or a linked list of free locations in CPU memory (Ramakrishnan, col. 2, lines 63-65).

Therefore, it would have been obvious to combine Aipperspach and Ramakrishnan for the benefit of obtaining the invention as specified in claim 1.

12. **As per claim 21**, Aipperspach discloses a memory manager comprises:

a process to allocate a memory entry in a memory device to instructions executed on a multithreaded engine (col. 1, lines 33-40; col. 3, lines 44-47; col. 5, lines 31-32; Fig. 3).

Aipperspach does not expressly disclose a packet processor and a portion of the memory entry includes a unique identifier assigned to the instructions.

Ramakrishnan discloses a packet processor and a portion of the memory entry includes a unique identifier (col. 4, lines 21-22 and 52-61; Fig.1, element 106; Fig. 2, element 220).

13. **As per claim 24**, Aipperspach discloses a system comprising:

a packet processor capable of, allocating a memory entry in a memory device to instructions executed on a multithreaded engine (col. 1, lines 33-40; col. 3, lines 44-47; col. 5, lines 31-32; Fig. 3).

Aipperspach does not expressly disclose a packet processor and a portion of the memory entry includes a unique identifier assigned to the instructions.

Ramakrishnan discloses a packet processor and a portion of the memory entry includes a unique identifier assigned to the instructions (col. 4, lines 21-22 and 52-61; Fig.1, element 106; Fig. 2, element 220).

14. **As per claim 27**, Aipperspach discloses allocating a memory entry in a memory device to instructions executed on a multithreaded engine (col. 1, lines 33-40; col. 3, lines 44-47; col. 5, lines 31-32; Fig. 3).

Aipperspach does not expressly disclose a network forwarding device comprising:

an input port for receiving packets;

an output for delivering the received packets;

a network processor and a portion of the memory entry includes a unique identifier assigned to the instructions.

Ramakrishnan discloses a network forwarding device comprising:

an input port for receiving packets (col. 4, lines 4-12; Fig. 1, element 102). It should be noted that "frames" are analogous "packets." It should also be noted that in order for the "PHY" to identify incoming Ethernet frames it is inherently required the "PHY" has an input port for receiving packets.

an output for delivering the received packets (col. 4, lines 47-48). It should be noted that in order for the "switch fabric" to create a datapath between two packet processors it is inherently required the "switch fabric" has an output port for delivering packets from one processor to the other processor.

a network processor and a portion of the memory entry includes a unique identifier assigned to the instructions (col. 4, lines 21-22 and 52-61; Fig.1, element 106; Fig. 2, element 220).

15. **As per claim 30**, Aipperspach discloses a method comprising:

allocating a content-addressable-memory (CAM) entry to a microblock executed on a multithreaded microengine (col. 4, lines 21-22 and 52-61; col. 10, lines 26-31; Fig.1, element 106; Fig. 2, element 220). It should be noted that "multiple threads" are analogous to a "microblock."

Aipperspach does not expressly disclose a network processor and a portion of the CAM entry includes a unique identifier assigned to the microblock.

Ramakrishnan discloses a network processor and a portion of the CAM entry includes a unique identifier assigned to the microblock (col. 4, lines 21-22 and 52-61; Fig.1, element 106; Fig. 2, element 220).

16. Claims 2, 4-5, 12, 14-15, 22, 25, 28, 31 are rejected under 35 U.S.C. 103(a) as being obvious over Aipperspach in view of Ramakrishnan as applied to claims 1, 21, 24, 27, and 30 above, and further in view of Pereira et al. (U.S Patent 6,697,276).

17. **As per claims 2 and 12**, Aipperspach/Ramakrishnan discloses a multithreaded engine (see citation for claim 1 above).

Aipperspach/Ramakrishnan does not expressly disclose maintaining a count of threads that use the memory entry.

Pereira discloses maintaining a count of threads that use the memory entry (col. 56, lines 27-34).

Aipperspach/Ramakrishnan and Pereira are analogous art because they are from the same field of endeavor, that content addressable memory (CAM).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Pereira's fill counter to monitor the activity of Aipperspach/Ramakrishnan's CAM entries.

The motivation for doing so would have been to achieve a significantly higher memory density in a hash CAM device and also use significantly less power to search a hash CAM device (Pereira, col. 4 line 67 – col. 5, line 6).

Therefore, it would have been obvious to combine Aipperspach/Ramakrishnan and Pereira for the benefit of obtaining the invention as specified in claim 2.

18. **As per claims 4 and 14**, Pereira discloses maintaining the count includes incrementing the count to represent a thread initiating use of the memory entry (col. 56, lines 27-30). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify what determines "initiating use of the memory entry." Pereira discloses insertion of a CAM entry, thus, "initiating use of a CAM entry."

19. **As per claims 5 and 15**, Pereira discloses maintaining the count includes decrementing the count to represent a thread halting use of the memory entry (col. 56, lines 30-34). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify what determines

"halting use of the memory entry." Pereira discloses deletion of a CAM entry, thus, "halting use of a CAM entry."

20. **As per claim 22**, Aipperspach/Ramakrishnan discloses a multithreaded engine (see citation for claim 21 above).

Aipperspach/Ramakrishnan does not expressly disclose a process to maintain a count of threads that use the memory entry.

Pereira discloses a process to maintain a count of threads that use the memory entry (col. 56, lines 27-34).

21. **As per claim 25**, Aipperspach/Ramakrishnan discloses a packet processor (Ramakrishnan, col. 4, lines 21-22; Fig. 1, element 106) and a multithreaded engine (see citation for claim 24 above).

Aipperspach/Ramakrishnan does not expressly disclose maintaining a count of threads that use the memory entry.

Pereira discloses maintaining a count of threads that use the memory entry (col. 56, lines 27-34).

22. **As per claim 28**, Aipperspach/Ramakrishnan discloses a network processor (Ramakrishnan, col. 4, lines 21-22; Fig. 1, element 106) and a multithreaded engine (see citation for claim 27 above). It should be noted that "packet processor" is analogous to "network processor."

Aipperspach/Ramakrishnan does not expressly disclose maintaining a count of threads that use the memory entry.

Pereira discloses maintaining a count of threads that use the memory entry (col. 56, lines 27-34).

23. **As per claim 31**, Aipperspach/Ramakrishnan discloses a multithreaded microengine included in a network processor (see citation for claim 30 above).

Aipperspach/Ramakrishnan does not expressly disclose maintaining a count of threads that use the CAM entry.

Pereira discloses maintaining a count of threads that use the CAM entry (col. 56, lines 27-34).

24. Claims 3, 6-10, 13, 16-20, 23, 26, 29, and 32 are rejected under 35 U.S.C. 103(a) as being obvious over Aipperspach in view of Ramakrishnan as applied to claims 1, 21, 24, 27, and 30 above, and further in view of Litt et al. (U.S Patent Application Publication 2003/0126358).

25. **As per claims 3 and 13**, Aipperspach/Ramakrishnan discloses all the limitations of claim 3 except maintaining a bit to represent availability of the memory entry for thread use.

Litt discloses maintaining a bit to represent availability of the memory entry for thread use (paragraph 0035, lines 7-9; Fig. 1, element 170). It should be noted that the "output of the AND gate" is either a high or low voltage. A bit is represented physically by either a high or low voltage. Therefore, the "output of the AND gate" is analogous to a "bit."

Aipperspach/Ramakrishnan and Litt are analogous art because they are from the same field of endeavor, that content addressable memory (CAM).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Litt's valid bit within Aipperspach/Ramakrishnan's CAM entry.

The motivation for doing so would have been to have a technique which permits software loops to be detected and eliminates multiple iterations of a software loop from being stored in memory as part of a PC trace, thus, reducing memory consumption (Litt, paragraph 0018, lines 1-4).

Therefore, it would have been obvious to combine Aipperspach/Ramakrishnan and Litt for the benefit of obtaining the invention as specified in claim 3.

26. **As per claims 6 and 16**, Litt discloses maintaining the bit includes setting the bit to represent availability of the memory entry for thread use (paragraph 0036, lines 25-32).

27. **As per claims 7 and 17**, Litt discloses maintaining the bit includes clearing the bit to represent unavailability of the memory entry for thread use (paragraph 0036, lines 32-38).

28. **As per claims 8 and 18**, Litt discloses checking the bit to determine the availability of the memory entry for thread use (paragraph 0035, lines 7-9).

29. **As per claims 9 and 19**, Litt discloses the unique identifier includes four bits (paragraph 0037, lines 4-5; paragraph 0038, lines 26-27). It should be noted that "Mask signal" is analogous to "unique identifier."

30. **As per claims 10 and 20**, Aipperspach/Ramakrishnan discloses a multithreaded engine of the packet processor (see citations for claim 1 above).

Aipperspach/Ramakrishnan does not expressly disclose the memory entry identifies a location in a local memory.

Litt discloses the memory entry identifies a location in a local memory (paragraph 0019, lines 4-8). It should be noted that "instruction address" is analogous to "identifier of a location in a local memory."

31. **As per claim 23**, Litt discloses a process to maintain a bit to represent availability of the memory entry for thread use (paragraph 0035, lines 7-9; Fig. 1, element 170).

32. **As per claim 26**, Aipperspach/Ramakrishnan discloses a network processor (Ramakrishnan, col. 4, lines 21-22; Fig. 1, element 106). It should be noted that "packet processor" is analogous to "network processor."

Aipperspach/Ramakrishnan does not expressly disclose maintaining a bit to represent availability of the memory entry for thread use.

Litt discloses maintaining a bit to represent availability of the memory entry for thread use (paragraph 0035, lines 7-9; Fig. 1, element 170).

33. **As per claim 29**, Aipperspach/Ramakrishnan discloses a network processor (Ramakrishnan, col. 4, lines 21-22; Fig. 1, element 106).

Aipperspach/Ramakrishnan does not expressly disclose discloses maintaining a bit to represent availability of the memory entry for thread use.

Litt discloses maintaining a bit to represent availability of the memory entry for thread use (paragraph 0035, lines 7-9; Fig. 1, element 170).

34. **As per claim 32**, Litt discloses maintaining a bit in a status register to represent availability of the CAM entry to identify a local memory location (paragraph 0038, lines 3-5; Fig. 2, element 250).

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

The following references disclose various **systems and methods relating to content addressable memory (CAM)**.

U.S. Patent Number

5,574,875

5,819,308

6,122,706

6,226,710

6,324,624

6,473,846

6,480,931

6,661,686

6,779,043

6,820,170

U.S. Patent Application Publication Number

2002/0032681

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-32** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
December 19, 2005

DONALD SPARKS
SUPERVISORY PATENT EXAMINER